AMENDMENT TO SPECIFICATION

IN THE SPECIFICATION:

A marked-up copy of the changes to selected paragraph(s) is provided below. Please enter these changes to the specification in the record.

Please amend Paragraph [0011] as follows:

> FIGS. 2[[(a)]] through 2(l) illustrate an exemplary process for forming a transistor according to the invention;

Please amend Paragraph [0034] as follows:

> After salicidation is completed, in the methods according to this invention an etch stop nitride film 245 is deposited over the wafer, as shown in FIG. 2(k). The film may be of tensile stress or compressive stress. Depending on the topography of the shallow-trench-isolation oxide (STI) which surrounds and/or isolates one device from another device, the stress level induced in the transistor channel may be changed. Thus, by adjusting the thickness of the shallow-trench-isolation oxide which is adjacent to and/or isolates one device from the others (as shown in FIG. 2), it is possible to adjust the stress level in the corresponding transistor channel such that the desired stress type (i.e., compressive or tensile) is formed therein.

Please amend Paragraph [0036] as follows:

In the methods according to this invention because the source and drain regions of the semiconductor device are formed on portions of the semiconductor substrate which are undisturbed (i.e., not etched and re-formed), the surface is more favorable to cobalt silicide formation as cobalt silicide. Further, in the methods according to this invention, the thickness of the STI oxide of a transistor is ~~be~~ adjusted and/or the distance of the STI oxide from the channel of the transistor is adjusted so as to control the amount and type of strain (i.e., compressive strain or tensile strain) created in the channel of the transistor. In particular, as further discussed below, by providing an STI oxide with a first thickness around the NFETs and providing an STI oxide with a second thickness around the PFETs (as shown in FIG. 2), it is possible to prevent the formation of the "undesired" (i.e., tensile stress in the PFET and compressive stress in the NFET) and even form the desired stress (i.e., compressive stress in the PFET and tensile stress in the NFET) with a same stress/strain layer for both the NFETs and the PFETs.